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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HOGAN, MARY C	
ART UNIT	**PAPER NUMBER**
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/779,859	KITAJIMA ET AL.	
	Examiner	Art Unit	
	Mary C Hogan	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This application has been examined.

2. **Claims 1-12** have been examined and rejected.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file, specifically, Japanese Patent Application Number 2000-032335, filed 02/09/2000.

Specification

4. The abstract of the disclosure is objected to because **(page 1, line 3)** the comma after "which value" should be removed. Correction is required. See MPEP § 608.01(b).

5. **Page 1, Line 11**: "there are known" should be changed to "there is known".

6. **Page 1, Line 14**: "and so on" should be deleted.

7. **Page 2, Line 12**: the comma after value should be deleted.

8. **Page 2, Line 14**:"a" should be deleted.

9. **Page 2, Lines 14-15, page 3, Line 20-21, page 8, Lines 14-15, 19-20**, "Log_2 a raised integer of (the specifying value)" and similar statements are unclear in meaning and should be changed to be in equation form further specifying definitions for the variables.

Claim Objections

10. **Claims 1,5,7,8, and 11** are objected to because of the following informalities. Appropriate correction is required.

11. **Claim 1**: "emulating a logic" should read "emulating logic", "synthesizing a multi-value" should read "synthesizing multi-value".

12. **Claims 5, 8 and 11**: In **Claim 5**, "Log_2 a raised integer of (the specifying value)" does not define what the variable "a" is. In **Claims 5,8 and 11**, "raised integer of" is grammatically incorrect. The equation in these claims should be changed to be of mathematical equation form, specifying definitions of the variables.

13. **Claim 7**: "emulating a logic" should read "emulating logic" or "emulating a logic circuit".

Claim Interpretation

14. **Claims 5,8 and 11** are directed to: "Log_2 a raised integer of (the specifying value)" and "Log_2 raised integer of (the specifying value)". **Claim 5** is directed to calculating the number of *logic* signals and **Claims 8 and 11** are directed to calculating the number of *physical* signals, which make the claims unclear as to what they are directed to. It has been concluded that the claims are directed to calculating the number of *physical* signal lines and the formula for this is "$\log_2 a = k$" where "a" is the value of logic being implemented and "k" is the number of physical signal lines needed to implement one logic signal.

Claim Rejections - 35 USC § 112

15. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

16. **Claims 1-12** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification broadly refers to multi-value supporting logic, logic value, physical signal lines, multi-valued logic signal, multi-valued synthesis, and "$\log_2$a raised to the integer of the specifying value". However, the specification does not provide any substantive detail, other than broad reference, to these concepts in such a manner to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

17. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

18. **Claims 5,8, 11 and 12** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

19. **Claim 5** states "Log_2 a raised integer of (the specifying value)" but does not define what the variable "a" is. Further, **Claim 5** is directed to "calculates the number of *logic* signal lines in a logic circuit" where the specification **(pages 2 and 8)** states that this equation is directed to determining the number of *physical* signal lines, making the claim vague and indefinite.

20. **Claims 8 and 11** state "Log_2 Raised Integer of Value Information", but do not include a variable "a". It is unclear if the equations in **Claims 8 and 11** are equivalent or not to the equation in **Claim 5** and to the equations stated in the specification **(page 2 lines 14-15, page 8 equation 1)**. Further, these claims are directed to "calculates a required number of *physical* signal lines" whereas the specification **(page 3, lines 19-21)** states that this equation is used to calculate the number of *logic* signal lines. These claims are vague and indefinite for these reasons.

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

23. **Claims 1,2,4-6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin at al (U.S. Patent Number 6,389,379), herein referred to as **Lin**, further in view of Lindgren et al (Lindgren et al, "Look-up-Table FPGA Synthesis from Minimized Multi-Valued Pseudo Kronecker Expressions"

Proceedings of the 28th IEEE Symposium on Multiple-Valued Logic, pages 95-100, 1998), herein referred to as **Lindgren**.

24. As to **Claim 1**, **Lin** teaches a logic emulation system for emulating a logic under verification, comprising: a synthesis unit for synthesizing logic under verification **(column 33, lines 43-54)**, a logic compile unit for assigning logic to a programmable gate array **(column 34, lines 37-51)** and an emulation unit for performing logic emulation using the programmable gate array **(column 18, line 63-column 19, line 4)**.

25. **Lin** does not expressly teach the synthesis unit synthesizing multi-value supporting logic.

26. **Lindgren** teaches a multi-value synthesis methodology that employs multi-valued expressions that restrict logic minimization to consider only easily mappable expressions, thereby forming a lay-out structure without routing overhead **(Abstract and page 1, column 2, second paragraph)** since tools have been developed in the past that minimize Boolean functions and map them to FPGAs, considering logic minimization, mapping and routing independently, but suffer from large area overhead in cases where the highly optimized netlists do not fit well on the target FPGA **(Section 1, first paragraph)**.

27. As to **Claim 2**, **Lin** teaches a synthesis unit **(column 33, lines 43-54).**

28. **Lin** does not expressly teach said synthesis unit implements one logic signal line for transmitting a multi-valued logic signal by a plurality of physical signal lines to synthesize the logic.

29. **Lindgren** teaches synthesis implementing one logic signal line for transmitting a multi-valued logic signal by a plurality of physical signal lines to synthesize the logic **(Section 3.2, first sentence where k is the number of physical signal lines needed to synthesize the logic)**.

30. As to **Claim 4**, **Lin** teaches said synthesis unit performs logic synthesis using information on a logic cell stored in a cell library **(column 33, lines 43-54)**.

31. As to **Claim 5**, **Lin** does not expressly teach said synthesis unit reads a specifying value that specifies with which value the synthesis is performed, and calculates the number of physical signal lines needed to logically connect the respective signal lines as $\text{Log}_2\ a = k$.

32. **Lindgren** teaches a synthesis method that calculates the number of physical signal lines needed to logically connect the respective signal lines as $\text{Log}_2\ a = k$ **(section 3.2, first two sentences in which the value of synthesis, v, to be performed must be known to determine k)**.

33. As to **Claim 6**, **Lin** teaches said system performs one logic gate operation using a programmable device in said programmable gate array in a multiple-input/one-output or multiple-input/multiple output configuration **(column 18, lines 39-41, column 33, lines 53-54 and column 62 lines 43-56)** where it is discussed that two four-input LUT's provide some of the inputs to a third three-input lookup table.

34. It would have been obvious to one of ordinary skill in the art at the time of the present invention to modify the synthesis unit as taught in **Lin** with the multi-valued synthesis methodology as taught in **Lindgren** since employing multi-valued expressions restrict logic minimization to consider only mappable expressions, thereby reducing routing overhead on FPGAs as taught in **Lindgren (Section 1, first paragraph)**.

35. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Lin** and **Lindgren** as applied to **Claim 1** above, and further in view of Yurchak (Yurchak et al, "HAMLET-An Expression Compiler/Optimizer for the Implementation of Heuristics to Minimize Multiple-Valued Programmable Logic Arrays", Proceedings of the 20th IEEE Symposium on Multiple-Valued Logic, pages 144-152, 1990), herein referred to as **Yurchak.**

36. As to **Claim 3**, **Lin** and **Lindgren** teach a logic emulation system comprising a synthesis unit **(see paragraph 24)** and performing multi-valued synthesis corresponding to a value of the logic **(see paragraphs 31-32)**.

37. **Lin** and **Lindgren** do not expressly teach the synthesis unit including a value storage unit for storing value information.

38. **Yurchak** teaches a synthesis unit including a value information storage unit for storing value information **(page 147, first two sentences under Figure 2 and Figure 3, "radix = 4" and "#var = 2)** and performs multi-valued synthesis corresponding to a value stored in said value information storage unit **(page 147, column 1, last 5 sentences)**.

39. It would have been obvious to one of ordinary skill in the art at the time the invention was made to store the value of synthesis as taught in **Lin** and **Lindgren** in a value information storage unit as taught in **Yurchak** since the value of logic must be stored in a storage unit in order for the necessary computations to be made for synthesis.

40. **Claims 7-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Lin** in view of **Lindgren** and further in view of **Yurchak**.

41. As to **Claims 7-9**, **Lin** teaches a logic emulation system including a plurality of writable logic devices **(column 16, lines 50-55 and column 18, line 63-column19, line 4)**, said system having an information processing unit reading information of a logic circuit to be emulated **(Figure 1, element 10 and description)**, a processing unit for mapping and compiling said logic circuit **(column 33, lines 43-54, column 34, lines 38-51)**, and a storage unit for storing information on a logic circuit under emulation **(Figure 1, element 15 and description)**.

42. **Lin** does not expressly teach the emulation system as emulating multi-valued logic including the processing unit calculating a required number of physical signal lines from said logic circuit information and said value information as Log_2 a = k.

43. **Lindgren** teaches a multi-value synthesis methodology that employs multi-valued expressions that restrict logic minimization to consider only easily mappable expressions, thereby forming a lay-out structure without routing overhead **(Abstract and page 1, column 2, second paragraph)** since tools have been developed in the past that minimize Boolean functions and map them to FPGAs, considering logic minimization, mapping and routing independently, but suffer from large area overhead in cases where the highly optimized netlists do not fit well on the target FPGA **(Section 1, first paragraph)**.

44. Further, **Lindgren** teaches the processing unit calculating a required number of physical signal lines from said logic circuit information and said value information as Log_2 a = k **(section 3.2, first two sentences in which the value of synthesis to be performed must be known to determine k)**.

45. It would have been obvious to one of ordinary skill in the art at the time of the present invention to modify the emulation system as taught in **Lin** to perform multi-valued emulation using the methodology as taught in **Lindgren** since employing multi-valued expressions restrict logic minimization to consider only mappable expressions, thereby reducing routing overhead on FPGAs as taught in **Lindgren (Section 1, first paragraph)**.

46. Lin teaches a storage unit for storing information on a logic circuit under emulation **(Figure 1, element 15 and description)** and an input device (column 23, lines 19-23).

47. **Lin** does not expressly teach the storage unit storing value information on a logic value of said logic circuit or the input device for inputting value information.

48. **Yurchak** teaches a storage unit for storing information on a logic circuit under emulation **(page 147, first two sentences under Figure 2 and Figure 3, "radix = 4" and "#var = 2).** Further, **Yurchak** teaches the input device for inputting value information **(page 147, Section IV, paragraph B, wherein the user creates an input file consisting of multiple valued logic expressions that define the value of logic)**.

49. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the storage unit as taught in **Lin** to store value information for a logic circuit as taught in **Yurchak** if the emulation system as taught in **Lin** is used to perform multiple-value logic emulation.

50. **Claims 10-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yurchak** in view of **Lindgren** in further view of **Lin**.

51. As to **Claims 10-12, Yurchak** teaches information processing unit reading information of a logic circuit to be emulated acquiring value information using an input device **(page 147, Section IV, paragraph B, wherein the user creates an input file consisting of multiple valued logic expressions that define the value of logic)** and storing value information on a logic value **(page 147, first two sentences under Figure 2 and Figure 3, "radix = 4" and "#var = 2),** and creating a multi-valued logic emulation program for said logic circuit **(page 151, paragraph E, first sentence)**.

52. **Yurchak** teaches expressing the functionality of logic circuits in the information processing unit as sum-of-products expressions as an alternative to a truth table representation **(page 144, paragraph 1, lines 5-8)**.

53. **Yurchak** does not expressly teach the processing unit calculating a required number of signal lines from said logic circuit information as Log_2 a = k consistent with a look up table or truth table representation.

54. **Lindgren** teaches a logic synthesis method applicable to look up table representations, the processing unit calculating a required number of physical signal lines from said logic circuit information and said value information as Log_2 a = k **(section 3.2, first two sentences in which the value of synthesis to be performed must be known to determine k)**.

55. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the processing unit in **Yurchak** with the information processing unit in **Lindgren** since a look up table, or truth table representation is an alternative to the sum-of-products representation of a logic circuit as taught in **Yurchak (page 144, paragraph 1, lines 5-8)**.

56. **Yurchak** teaches producing a layout file for a multiple-valued programmable logic array **(page 151, paragraph E, first sentence)**.

57. **Yurchak** does not expressly teach emulation including a plurality of programmable logic devices.

58. Lin teaches emulation including a plurality of programmable logic devices **(column 16, lines 50-55 and column 18, line 63-column19, line 4)** wherein a logic compile unit for assigns logic to a programmable gate array **(column 34, lines 37-51)** and an emulation unit for performs logic emulation using the programmable gate array **(column 18, line 63-column 19, line 4).**

59. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the layout file as taught in **Yurchak** to map to a plurality of programmable logic devices and perform emulation as taught in **Lin** since emulation is used to verify the design in hardware form in its

target environment **(column 4, lines 4-7)** and is recognized as a valuable tool in various industries that use electronic design automation as taught in **Lin (column 1 lines 33-35).**

Conclusion

60. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

61. Sheikholeslami et al (Sheikholeslami et al, "Look-Up Tables (LUTs) for Multiple-Valued, Combinational Logic", Proceedings of the 28th IEEE Symposium on Multiple-Valued Logic, pages 264-269, 1998), teaches the use of look up tables for multiple-valued logic.

62. Miller, D. Michael, (Miller, D. Michael, "Multiple-Valued Logic Design Tools", Proceedings of the 23rd IEEE Symposium on Multiple-Valued Logic, pages 24-27, 1993), teaches multiple-valued logic design with respect to multiple-valued field programmable gate arrays.

63. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C Hogan whose telephone number is 703-305-7838. The examiner can normally be reached on 7:30AM-5PM Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary C Hogan
Examiner
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KEVIN J. TESKA
SUPERVISORY
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